ABSTRACT OF THE DISCLOSURE

A clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof is provided in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal. The recording medium is recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic. The clock adjustment apparatus includes a phase error calculation circuit which calculates the phase error of the clock signal based on the sampled values of the readout signal.